REMARKS

As suggested by the Examiner, a replacement drawing sheet for Figure 1 is supplied with this amendment. Acknowledgment of receipt and acceptance of the replacement drawing sheet is respectfully requested.

The specification was objected to as failing to provide proper antecedent basis for the claimed subject matter of claims 14 and 16.

As to claim 14, the Examiner states that the specification fails to provide support for the limitation "after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units." Support for this limitation is found on page 9, lines 29–33. Moreover, the original claim language constitutes part of the original disclosure. Withdrawal of the objection on this ground is respectfully requested.

With respect to claim 16, the Examiner states that "The specification fails to provide the support for 'data load' or '**data load and** network characteristic'." (emphasis the Examiner's) In the first Office Action mailed May 29, 2007, the Examiner objected to the specification for failing to provide proper antecedent basis for the claimed subject matter of claim 1. Specifically, claim 1 recited "changed **data rates**" in line 7, but there is no support for "data rate" in the specification. As described in the amendment filed August 29, 2007, the intent of the disclosed and claimed invention is to base the decision either on changed data rate (of the sender) or network load (which is called "network characteristics"). Accordingly, the specification was amended to more accurately reflect this intent than in the original German translation. Claim 16 has been amended in this paper to reflect the amendment made to the specification in the prior amendment; i.e., "data load" has been changed to –data rate–. This amendment is believed to overcome the objection.

Claims 1 to 18 remain in the application. Claims 1, 2 and 16 are amended by this amendment.

Claims 1 to 18 were objected to for informalities noted by the Examiner with respect to claims 1 and 2. The suggested amendments have been made to claims 1 and 2 and, therefore, withdrawal of the objection to the claims is respectfully requested.

Claims 13 and 14 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enabling requirement. As to claim 13, the Examiner contends that "the specification fails to disclose how subcomponents (see FIG. 3, 6a',6b',6c') of processing unit 3 are de-attached after switching to processing unit 4." The Examiner acknowledges that a response was provided in the prior amendment by citation to page 9, lines 29–33, but continues to ask questions which would not be asked by one of ordinary skill in this art. In describing the switch (switches 5 and 8 of Figure 3), the specification states on page 7, lines 27 and 28, that "The switch can hereby be realized as hardware or software." By implication, and as would be clearly understood by those of ordinary skill in the art, disconnection (and re-connection) of the codec, filter and packetizer could also be realized with either hardware or software switches.

As to claim 14, the Examiner ignores the clear recitation and meaning of the claim. What the claim recites is "a plurality of the second processing units" and that "the subcomponents of the first processing unit are included in one of the second processing units." Rather, the Examiner focuses on the embodiment illustrated in Figure 3 which shows only one second processing unit and asks how parallel processing can be done when the subcomponents of the first processing unit 3 are included in the second processing unit 4. The claim quite clearly contemplates a plurality of second processing units, and when the subcomponents of the first processing unit are incorporated into one of the second processing units, one of ordinary skill in the art would understand that parallel processing is performed by at least two of the plurality of second processing units.

Attached hereto is the declaration under 35 C.F.R. 1.132 of Koichi Funaya, an expert in the art of the disclosed and claimed invention. Mr. Funaya addresses the rejection of claims 13 and 14 under 35 U.S.C. §112, first paragraph, in numbered

paragraph 4 on page 3 of his declaration. First of all, in numbered paragraph 3 at the bottom of page 2 of his declaration, Mr. Funaya specifies the level of education and skill in the art one of ordinary skill in the art would have for the disclosed and claimed invention, a person of this level of skill being the criteria for disclosure required under Section 112, first paragraph. Mr. Funaya states that the switching process recited in claim 13 "is quite straight-forward" and "can be realized in many ways". As to claim 14, Mr. Funaya states that "the Examiner ignores the clear recitation and meaning of the claim." Specifically, Mr. Funaya states that the "claim refers to the variant, where some of the original subcomponents of the first processing unit will be used again as subcomponents in one of the chains in the 'plurality of the second processing units'." Mr. Funaya notes that this would allow for both resource-efficient and speed-efficient implementation.

Claims 1 to 4 and 6 to 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry et al. This rejection is respectfully traversed for the reason that the combination of Zahn and Sastry et al. neither discloses nor suggests the claimed invention.

The disclosed and claimed invention is directed to an apparatus for the processing and transmission of an "apparatus for the transmission of time-synchronous data from a sender to a receiver using a network", and in particular, the network contemplated by the inventors is the Internet where the time-synchronous data is packetized for transmission using the Internet Protocol (IP).

The Examiner continues to contend that "Zahn discloses an apparatus (see FIG.1,2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3–8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4–6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2, 4, 5, the video data is processed at

transmitter or receiver/customer; see page 9, last paragraph) . . ." On page 9 of Zahn, the apparatus 1 is described as being connected by a PCI bus 2 to a CPU of a personal computer. For the Examiner's benefit, PCI stands for Peripheral Component Interconnect, a bus standard designed by Intel for personal computers. See page 537, second definition, of *Newton's Telecom Dictionary*, 14th Ed. (1998), copy attached. In other words, the apparatus 1 is a processor board which is inserted into a PCI bus card slot inside a personal computer. Zahn describes Figure 3 as illustrating "temporally sequential data packets like those occurring in video processing". This is not the same thing as time-synchronous data. As described at the top of page 11 of Zahn, "video signal 50 has temporally discrete and sequential data packets, so-called frames 100. . . which have the constant temporal spacing T, . . ." Zahn goes on to describe that a first frame 101 is requested by the dispatcher program of the primary processor along the PCI bus 2 along the local bus 7 of the apparatus 1. This data packet 101 is then decompressed by the decoder 3. This data is clearly not time-synchronous. The data packets are temporarily sequential; that is, they following one another in a sequential order, but they are static (i.e., stored on hard disk) until requested by the dispatcher program. The last paragraph of page 9 of Zahn describes the internal components of the PCI card apparatus 1. The acronyms "MPEG" and "HDTV" respectively stand for Motion Picture Experts Group and High Definition Television (see pages 341 and 465, *Newton's Telecom Dictionary* by Harry Newton (1998), copies attached). MPEG is a video encoding scheme, and HDTV merely describes a type of television having a 16-to-9 aspect ratio and a prescribed pixel resolution. Non-linear video editors of the type Zahn describes implement MPEG video encoding on video frames that have resolutions meeting the HDTV definition.

Thus, contrary to the Examiner's contention, Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of that data using a network. On the contrary, Zahn discloses a video processor board for a personal computer (PC) for connection to the Peripheral Component Interconnect (PCI) bus. This video processor board is for non-linear video editing (NLE, see page

4, line 8, of Zahn) systems which, by their very nature, are not transmitting time-synchronous data from a sender to a receiver. The Zahn video processor board may include multiple processors, but their operation is entirely different from the claimed first and second processors. In the case of the Zahn video processor board, the multiple processors are for the purpose of improving rendering speed of the video data being edited. This process is not real time. In contrast, the first and second processing units of the claimed invention operate in a manner to avoid time delays and resulting dropping of frames in the transmission of the time-synchronous data. This is process is real time.

For further explanation of HDTV, NLE systems and video processing expansion cards, see the following attached articles from Wikipedia:

- High-definition television
- Non-linear editing system
- Video processing expansion card

At the heart of any NLE system is a video capture card which is inserted into an option card slot (currently a PCI or PCI express slot) in a PC. Attached is a copy of a paper entitled "Video 101" from ATI corporation, now merged with AMD corporation, which describes the fundamentals. Also attached is a copy of a product brochure for the Matrox RT.X2 system for professional NLE systems which includes a card, similar to the Zahn card, that is inserted into an option card slot of a PC. Home NLE systems are also commonly available, as indicated by the attached pages describing the Turtle Beach Video Advantage PCI video production system. The point here is that the claimed invention is not a NLE system of the Zahn type.

Mr. Funaya also addresses the Zahn reference in numbered paragraph 5 bridging pages 3 and 4 of his declaration under 37 C.F.R. 1.132. Mr. Funaya notes that "Zahn is directed to non-linear video editing which, by definition, is not time-synchronous transmission over a network."

The Examiner relies on Sastry et al. for a disclosure of "an apparatus (see FIG 1, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the

transmission of time-synchronous data (see FIG. 2, real time data; see col. 3, line 29–31, 48–51, 62–67) from a sender (see FIG. 2, sending/transmitting client 241–244/251–254) to a receiver (see FIG. 2, receiving client 251–254/241–244) using a network (see FIG. 2, using network 210), where in data is processed and transmitted to the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241–244 as well as the receiving client 251–254; see col. 3, line 32 to col. 4, line 10) . . ." What Sastry et al. actually disclose is a voice processing allocation scheme in an IP network to which multiple clients are connected via servers, as generally shown in Figure 2. The servers have processing modules 430 having multiple Digital Signal Processors (DSPs) 431 to 439. These DSPs implement various algorithms, such as Adaptive Differential Pulse Code Modulation (ADPCM) and Conjugated Structure Algebraic Code-Excited Linear Prediction (CS-ACELP) voice compression. These are processor intensive algorithms, and the problem addressed by Sastry et al. is the switching of active data connections from one processor to another processor without significantly interfering with the transmission of voice and other data. Sastry et al. do this using a DSP resource allocation algorithm to load share the data by selectively moving an active voice call currently being processed by one DSP to another DSP having sufficiently available processing power, without interrupting the prevailing service. The liberated DSP may then be used to process a new voice call. Figure 8 illustrates the data switching between DSPs. By load sharing among the DSPs, the number of simultaneous active voice calls supported by a voice processing module may be increased.

The DSP load sharing scheme of Sastry et al. is not the same or analogous to the claimed invention. In the claimed invention, adaptation to changed data rate and/or network characteristics has to be performed without further degradations of transmission quality. This is achieved through the setup of a parallel processing unit which is adapted to the changed data rate and/or network characteristics. This is not load sharing among a plurality of identical processors, as in Sastry et al. Rather, what the claimed invention does is to setup a parallel processor in which the individual

subcomponents of the parallel processor are adapted to the changed data rate and/or network conditions. Once the parallel processor is setup, that is, the subcomponents of the parallel processor are instantiated and initialized, processing and transmission of the time-synchronous data is performed by switching over to that processor by means of a switch.

Mr. Funaya discusses the rejection of claims 1 to 4 and 6 to 18 as being obvious in view of the Zahn and Sastry et al. references in numbered paragraph 7 beginning on page 4 and continuing to the top of page 6 of his declaration under 37 C.F.R. 1.132. Mr. Funaya notes again that claim 1 refers to a mechanism for the transmission of time-synchronous data, but Zahn does not transmit any data but operates on a single machine. As to claim 2, Mr. Funaya notes that this claim refers to the special case of necessity to change the parameters of the system during the transmission but that Zahn does not change the parameters the parameters of a video editing unit after setup. As to claim 3, Mr. Funaya notes that this claim refers to the idea of creating a connection to the second processing unit is only done when the setup and/or adaptation is already realized but that Zahn switches before setup since the timing problems of component setup time do not matter for video editing. Mr. Funaya notes that claims 6 to 18 refer to different variants of the core concept. Referring to the Sastry et al. patent, Mr. Funaya states "that in Sastry et al. all the processors are always active and perform processing operation in parallel" whereas "Applicants, on the other hand, disclose and claim a method whereby the second processing unit (or several units) is setup AFTER the switch command (which can't be known in advance in real time traffic and will be based on varying load conditions in the network or the clients)." Mr. Funaya goes on to say that "The claimed invention method ensures the DYNAMIC creation and deletion of processing chains, still no loss or interruption in the transmission will appear", whereas "Sastry et al. do not cover the problem of setup time at all."

To better emphasize the patentable novelty the invention, claim 1 is amended to recite

"a first processing unit composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous data in a specific and different way;

"a second processing unit parallel to the first processing unit, said second processing unit being composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous data in a specific and different way, wherein the subcomponents of the second processing unit are setup and adapted based on changed sender data rate or network characteristics by configuring attribute parameters of the subcomponents, wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit; and

"a switch selecting between the first and second processing units, the processing and transmission of the time-synchronous data initially being performed by the first processing unit and, after switching by the switch, the processing and transmission of the time-synchronous data is performed using the second processing unit such that the processing and transmission of the time-synchronous data is performed within the second processing unit."

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over the Zahn International Patent Publication and the Sastry et al. patent in view of U.S. Patent No. 7,095,717 to Muniere. This rejection is respectfully traversed for the reason that the combination of Zahn, Sastry et al. and Muniere does not teach, suggest or otherwise make obvious the claimed invention.

As discussed above, Zahn does not disclose the basic system recited in claim 1. The Zahn video processor board is for an entirely different function and is constructed and operates in a manner which is entirely different from the disclosed and claimed invention. The Sastry et al. load sharing scheme is not the same as the claimed setup of a parallel processor with subcomponents adapted for the changed data rate or network conditions. Muniere discloses a method for multiplexing two data flows on a radio communication channel and corresponding transmitter. Since

Zahn is not transmitting data from a sender to a receiver, Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields. Moreover, the claimed invention has nothing whatsoever to do with multiplexing two data flows. On the contrary, the claimed invention is concerned with the transmission of one data flow only, the time-synchronous data of, for example, video frames. Clearly there is no basis in fact for the conclusion of obviousness based on Zahn in combination with Sastry et al. and Muniere.

Mr. Funaya addresses the rejection of claim 5 in numbered paragraphs 8 and 9 on page 6 of his declaration under 37 C.F.R. 1.132. Mr. Funaya first of all notes that "Muniere proposes a multiplexing method to ensure prioritized transmission of high priority data with enough remaining bandwidth for the low priority data to flow." Mr. Funaya notes that "In real time transmission of multimedia data of packet networks, the transmission quality of the channel can vary quickly and significantly over time." Mr. Funaya states that "claim 5 specifies a solid method for the identification of an appropriate switching condition" and Muniere does not specify any conditions, since there is no switch involved in the Muniere multiplexing method. Moreover, neither Zahn nor Sastry et al. refer to the same decision as given in claim 5.

It is respectfully submitted that the claims have been misinterpreted by the Examiner. To aid the Examiner in his reconsideration of the claims, the following comments are offered. In the claimed invention, Applicants achieve seamless handovers between potentially many different (arbitrary complex) processing units as a mechanism for optimizing transmission quality in packet-based networks and low-power devices (e.g.., mobile telephones). The central idea is to allow adaption between various independent instantiations of processing units, as determined by a particular operating environment. Processing units may contain arbitrary complex subcomponents (codecs, filters, packetizers, etc.) and may be available locally within a device or downloaded by standard means over a network connection. Applicants claimed invention is novel in that it supports seamless adaption between the current operating processing chain and newly instantiated chains either by feeding data

simultaneously to both chains or utilizing additional processing resources for encoding within the second chain during setup.

In the claimed invention, Applicants switch the input of two or more independent processing units, where it is always guaranteed that only one of them is processing at any given time. In addition, Applicants coordinate the control sequence of parallel processing unit operations (setup, teardown or resource sharing) in order to minimize processing power requirements and allow the installation of potentially useful processing units specific to a given operational environment.

The features which characterize the claimed invention include the following:

- A digital media processing system with arbitrary number of "processing units".
- Generally applicable to real-time IP streaming media scenarios.
- Processing units are "not specified" and may include arbitrary chains of codecs, packetizers, etc.
- Seamless switching is intended to accommodate additional processing units (e.g., downloaded).
- Processing chain components may contain quality settings (e.g., quantizer settings).
- Processing chains are instantiated into memory "on-demand" by adaptation algorithms.
- Seamless switching refers to instantiating a processing unit and activating its input.
- Seamless switching does accommodate processing chain instantiation timing.
- Processing chains are never fed data simultaneously.
- Processing chains never operate on input data simultaneously.
- Seamless switching may include teardown or timed caching of unneeded processing units.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1 to 18 be allowed, and that the application be passed to

issue. In the alternative, it is requested that this amendment be entered for purposes of appeal.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Andreas Schrader and Darren Carlson
Serial No. 10/603,749
Filed June 26, 2003
For MECHANISM FOR TRANSMISSION OF TIME-SYNCHRONOUS DATA

Confirmation No. 3819
Group Art Unit 2616
Examiner Ian N. Moore

DECLARATION OF KOICHI FUNAYA
UNDER 37 C.F.R. 1.132

Koichi Funaya declares as follows:

1. During the period from April 1989 to April 2001, I was employed by NEC Central Research and NEC Home Electronics in the technical fields of robotics and mechanics, DSP (digital signal processing) for mechanical control applications, high-speed channels for storage systems, MPEG transcoding, and digital rights management. During the period from April 2001 to December 2004, I was employed by Network Development Labs, NEC Networks, Enterprise Solutions BU, Solutions Development Labs in the technical fields of multimedia contents design for Digital Terrestrial Broadcasting (ISDB-T), wireless access (WLAN) solutions for carriers and enterprise, and IMS based personal communication application "Push-to-X". During the period from January 2005 to June 2006, I was employed by Infineon Technologies in the fields of technical marketing and business development on wireless semiconductor products. Since June 2006, I have been employed by Network Research Division, NEC Laboratories Europe as CPO, Research Planning and Business Development.

I graduated from University of Tokyo with Bachelor of Science degree in Aerospace Engineering in 1987, from Massachusettes Institue of Technology with Master of Science degree in Aeronautics and Astronautics in 1988, and from University of Tokyo with Master of Science degree at the School of Engineering in 1989.

2. I have read and understood the subject patent application. Briefly described, the invention disclosed therein relates to a specification of a method which allows for changing components of a (real-time) media processing and/or transmitting chain in a seamless manner. This means, core elements of the processing system (e.g. a compressor) can be exchanged by an alternative component, without the need to interrupt the data flow as is common in current implementations of media adaptation. The main mechanism used is to provide the new system elements, before the old are removed and deleted. With this technique, the flow will not be interrupted at all and any loss can be avoided during this modification process. The positive aspect of this invention is that it can be realized in software and hardware. Based on the specific requirements of the application (e.g. video conference) or device (e.g. mobile phone), different realizations can be found. From my knowledge, the inventors used JMF for the prototype. But JMF has intrinsic timing problems. That might be the reason for the remaining time synchronization problems in video transmission. This could be easily avoided, if better suited programming languages, like C, will be used. For a mobile device, the implementation would of course be realized using electronic circuitry. As far as I can observe, existing chipsets could easily support the proposed method.

3. I have read and understood the Office Action mailed September 25, 2007, in the above-identified patent application. In my opinion, the Examiner is in error when he contends that claims 13 and 14 fail to comply with the enabling requirement of the U.S. Patent Statute. One of ordinary skill in the art to which the invention disclosed in the above-identified patent application is related would have a Bachelor or Master degree in electronic engineering, computer science, or a related field. Some experiments with programming media processing software would be helpful. But ordinary programming skills would be sufficient. For hardware implementations, knowledge in low-level hardware control software programming would be helpful.

4. In the above-identified patent application, the inventors specify in claim 13 as follows: "Mechanism according to claim 6, wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other". The switching process is quite straight-forward. The switch (8) in Fig. 3 is used to decide, which processing chain will receive data generated by one of the exemplified input generators (1). This can be realized in many ways. In JMF, it would mean to specify disconnecting the subcomponents are to be done automatically by JMF if a new connector (data sink) is decided for the original data source. In claim 13 nevertheless, the inventors definitely refer to the remaining subcomponents within the (disconnected) chain. Especially, if some subcomponents should be re-used for other purposes and in order to free resources, a dedicated disconnection will be helpful (e.g. JMF method "deallocate"). This would also release the implementation from additional performance requirements for synchronization and event-handling in all involved subcomponents. If other environments than JMF will be used, or if the process is realized in hardware, physical disconnection of subcomponents can be useful to avoid circuit feedback problems or to reduce energy consumption and heat problems. As to claim 14, the Examiner ignores the clear recitation and meaning of the claim. The claim refers to the variant, where some of the original subcomponents of the first processing unit will be used again as subcomponents in one of the chains in the "plurality of the second processing units". This would allow for resource-efficient implementation (in case of hardware) and speed-efficient implementation (in case of software). Especially, if the setup of a component would need some time to prepare operation, the re-use in the new processing chain ("... are included in one of the second ...") would avoid the waiting time for setting up an identical new subcomponent in the new chain. The inclusion would be realized by appropriate connectors (e.g. from switch 8 in fig. 3 to 7a of the new chain, 6b of the old chain and 7c of the new chain in order to re-use 6b).

5. I have read and understood International Patent Publication WO 00/62254 of Zahn relied on by the patent examiner. Briefly described, the Zahn reference relates to a method to organize video encoding using several processors AT THE SAME TIME. Zahn is

directed to non-linear video editing which, by definition, is not time-synchronous transmission over a network. Zahn proposes a system "in order to enable image processing at increased processing speed". The standard method would be to use several processors for calculation. Zahn mentions several drawbacks of this approach, which are mainly resulting from PCI bus overloading, since video frames or parts of video frames must be transported into main memory before processing. Other drawbacks are the additional overhead for the management, the limited scalability, and limitations of special rendering accelerators for uncompressed data transport speedup. The proposed mechanism is distributing data load in a smart way to several processing units, which operate independently on parts of the video signal.

6. I have read and understand U.S. Patent No. 6,694,373 to Sastry et al. The Sastry et al. reference relates to a mechanism to distribute processor load in a system of several DSPs or general processing chains which are able to handle several processes (streams) at the same time. Load balance is necessary to optimize the overall performance of the processor matrix within such a system.

7. In my opinion, the Examiner is in error in his rejection of the claims 1 to 4 and 6 to 18 as obvious in view of the Zahn and Sastry et al. references. Specifically, claim 1 refers to a mechanism for the transmission of time-synchronous data. Zahn does not transmit any data but operates on a single machine. Claim 2 refers to the special case of necessity to change the parameters of the system during the transmission. Zahn does not change the parameters of a video editing unit after setup. Claim 3 refers to the idea of creating a connection (switching) to the second processing unit is only done, when the setup and/or adaptation is already realized. Zahn switches before the setup, since the timing problems of component setup time do not matter for quasi-real time video editing. Claims 6 to 18 refer to different variants of the core concept. Multiple processing units could be setup in advance, if memory allows. This would reduce the switching time in case of adaptation. Zahn never switches any running processing chain, since he does not

consider any adaptation in a running chain or even complete process as soon as it is setup. Indeed, the processing chains in Zahn are also switched by a central unit in order to optimize the overall load, but no specific consideration is given to the problem of setup time of a component. The the contrary, Zahn does specifically accept a delay in setup. In page 12 Zahn states "... so that after a certain start up phase, a quasi-real time processing is achieved ... will there be a certain start up hesitation due to the calculation of the first data packets, which can be accepted."

In the subject invention of above-identified patent application, this setup time is not acceptable, since the invention deals with definitely real time processing and transmission, where no delay is acceptable. In Zhan, video editing on a single machine is optimized for load balancing between numerous processors. The claimed invention eliminates loss due to delays in setup of new processing chains (e.g. after codec) change in a running real time transmission session. Therefore, a similarity between the Zahn and the claimed invention can't be identified

Sastry et al. indeed use also different processing chains and a switch to decide which processor will handle the data processing within the stream (e.g. codec). The difference to the claimed invention of the above-identified patent application is the focus and detail of the switching method. Sastry et al. state themselves several times that the switching of active data from the first to the second processor is performed "... without significantly interfering ..." The main difference is, that in Sastry et al. all the processors are always active and perform processing operations in parallel. They are always ready to receive data for processing. The switch only decides which processor should get the data. The processor fetches the data of the respective stream out of a buffer which is fed by all streams served by this entity. Applicants, on the other hand, disclose and claim a method whereby the second processing unit (or several units) is setup AFTER the switch command (which can't be known in advance in real time traffic and will be based on varying load conditions in the network or the clients). Here the problem is that the new processing unit is not yet ready to perform during the setup phase. The claimed

invention method ensures that for DYNAMIC creation and deletion of processing chains, still no loss or interruption in the transmission will appear. Sastry et al. do not cover the problem of setup time at all.

8. I have read and understand U.S. Patent No. 7,095,717 to Muniere. Briefly described, the Muniere patent relates to a method for multiplexing two data flows in one communication channel. Specifically, Muniere deals with the problem of incoming data flows of different priorities. Muniere proposes a multiplexing method to ensure prioritized transmission of high priority data with enough remaining bandwidth for the low priority data flow.

9. In my opinion, the Examiner is in error in his rejection of claim 5 as being obvious over the combination of the Zahn, Sastry et al. and Muniere references. Claim 5 specifies the exact requirement for the switching condition in the described mechanism. "... whether at least one given parameter reaches at a predetermined value." In real time transmission of multimedia data of packet networks, the transmission quality of the channel can vary quickly and significantly over time. In order to adapt the processing parameters (e.g. of the codec, the packetizer, etc.) a complicated algorithm has to be defined in order to decide the optimum parameters based on measurement results or network feedback information. This algorithm, which is part of the proposed mechanism, will have to detect any change in any given parameter in order to decide the new parameter set. Therefore, claim 5 specifies a solid method for the identification of an appropriate switching condition.

None of the cited references specify this type of switch sensitivity to parameters. Muniere does not specify any conditions, since there is no switch involved. In Sastry et al. and Zahn, switching conditions might be defined, but they do not refer to the same decision as given in the above-identified patent application as stated above."

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

28.01.2008

Date

Kouichi Funaya